ABSTRACT OF THE DISCLOSURE

The present invention is generally directed to an apparatus and method for performing a partial flush of a processor pipeline in response to exceptions (e.g., interrupts). In accordance with an aspect of one embodiment a processor is provided with logic that operates to flush only limited stages of a processor pipepline (*e.g.*, stages between the current instruction and the pending interrupt) if the execution of a current instruction will impact the execution of a pending interrupt (*e.g.*, if the current instruction is a branch, if the current instruction would cause the processor to enter a mode that disables the pending interrupt, *etc.*). In accordance with another aspect of this embodiment, a method is provided for performing a partial flush of processor pipeline if the execution of a current instruction would impact the execution of a pending interrupt.